Parallel VID Communication

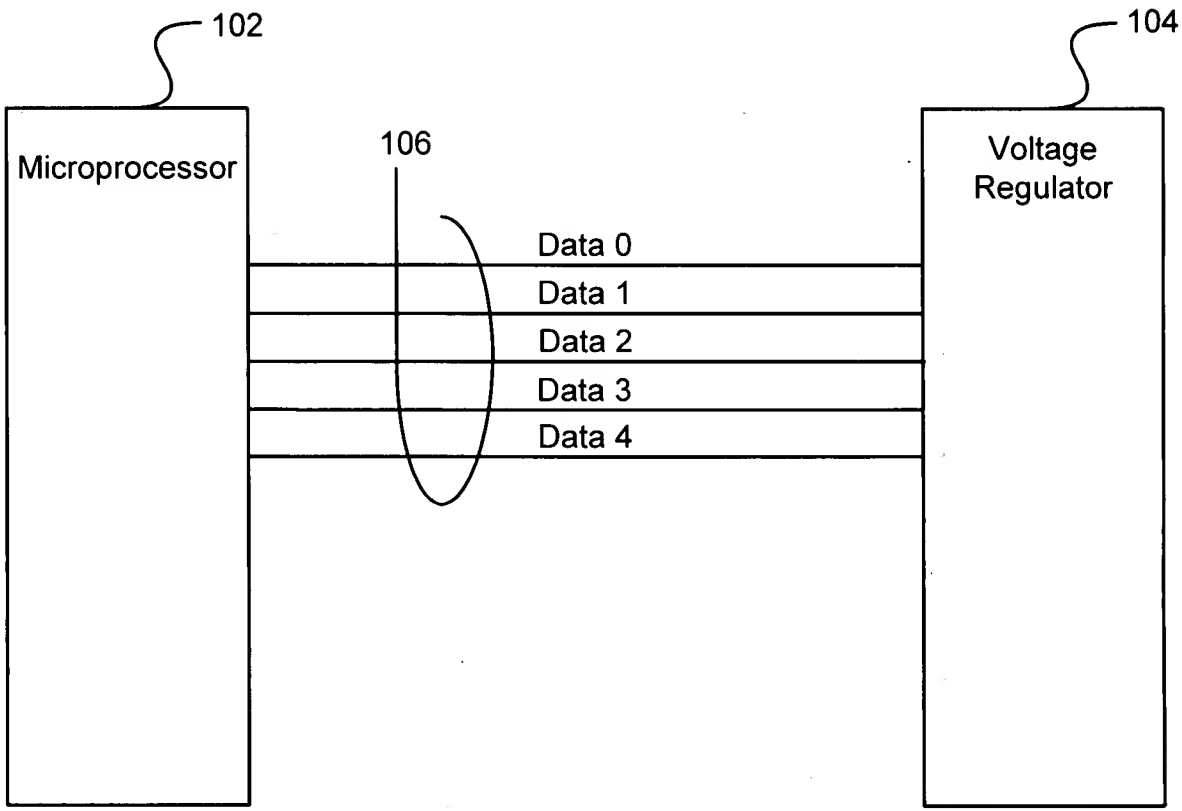

Fig. 1
Prior Art

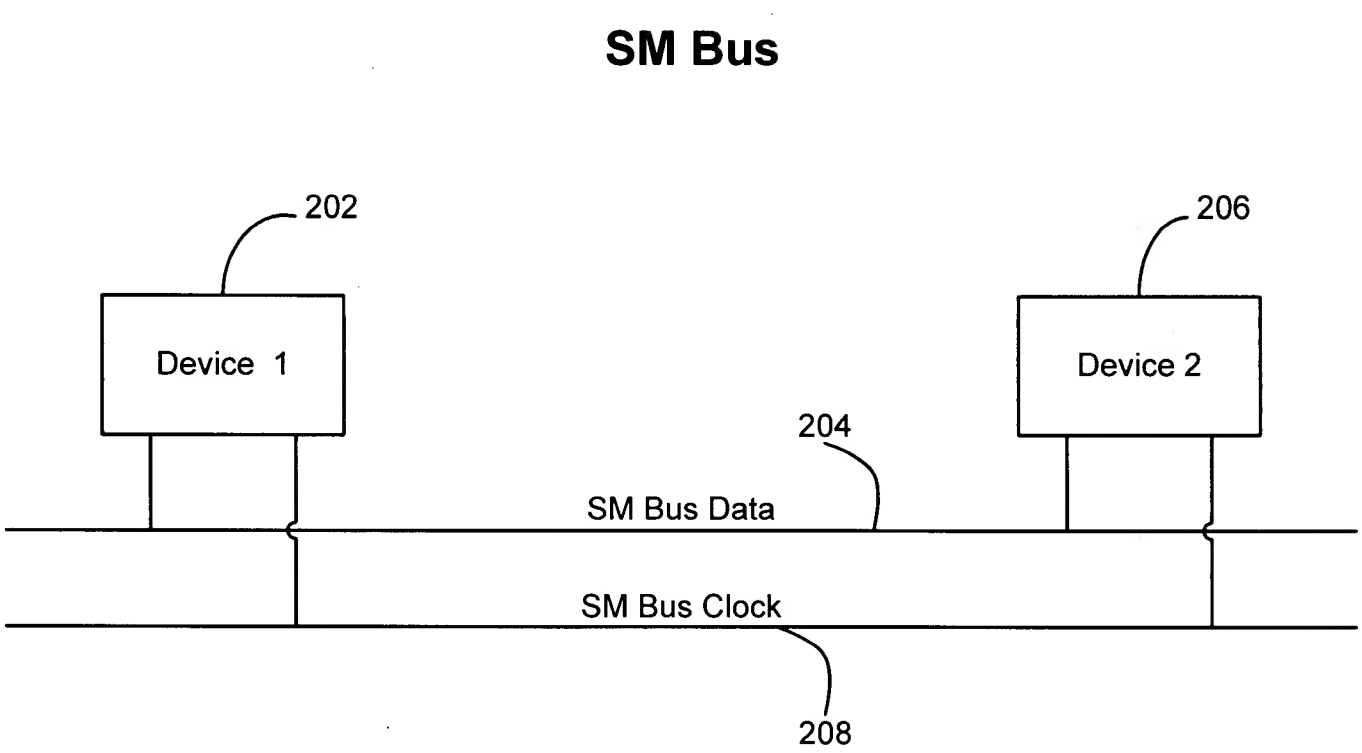

Fig. 2
Prior Art

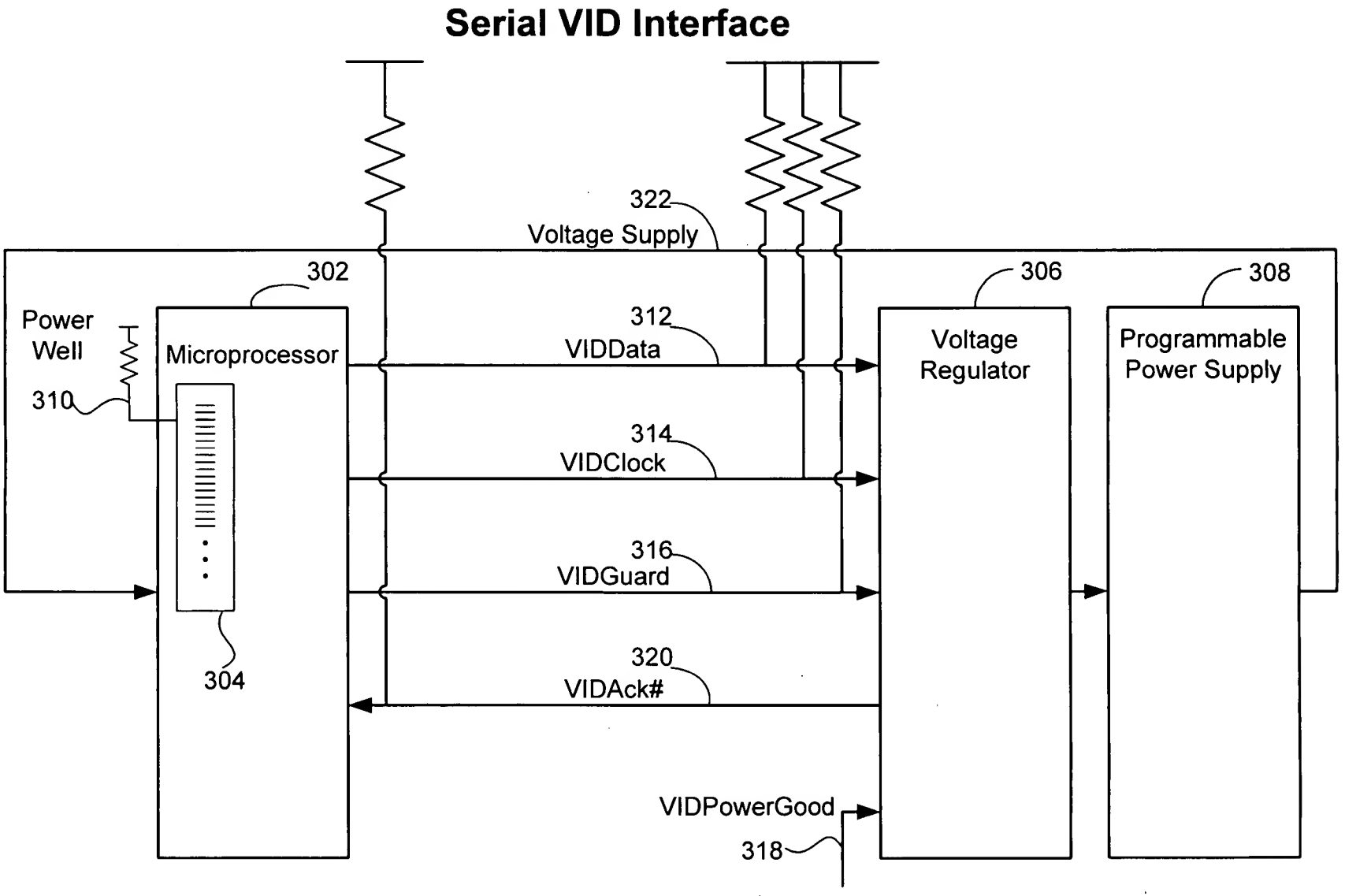
Serial VID Interface
322
Voltage Supply
302
306
308
Power
Well
310
Microprocessor
312
VIDData
Voltage
Regulator
Programmable
Power Supply
314
VIDClock
316
VIDGuard
304
320
VIDAck#
VIDPowerGood
318

Fig. 3

VIDData and VIDGuard Timing

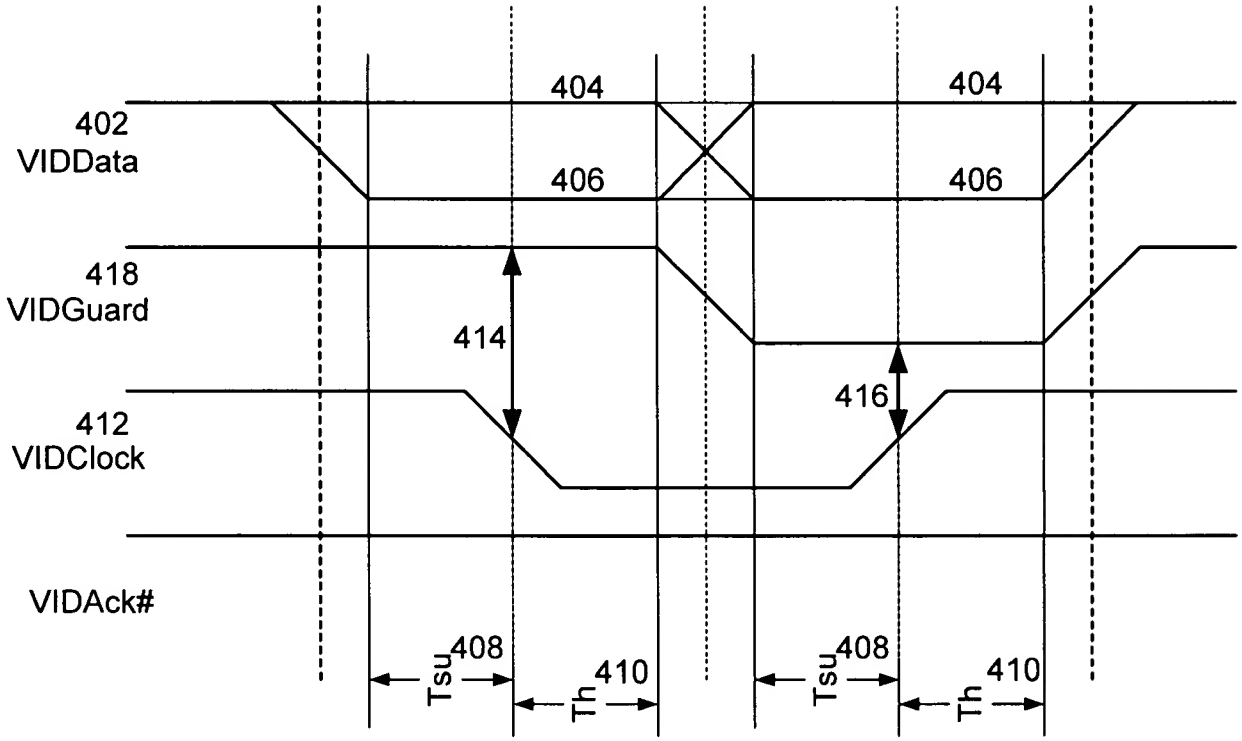

Fig. 4

VIDAck# Timing

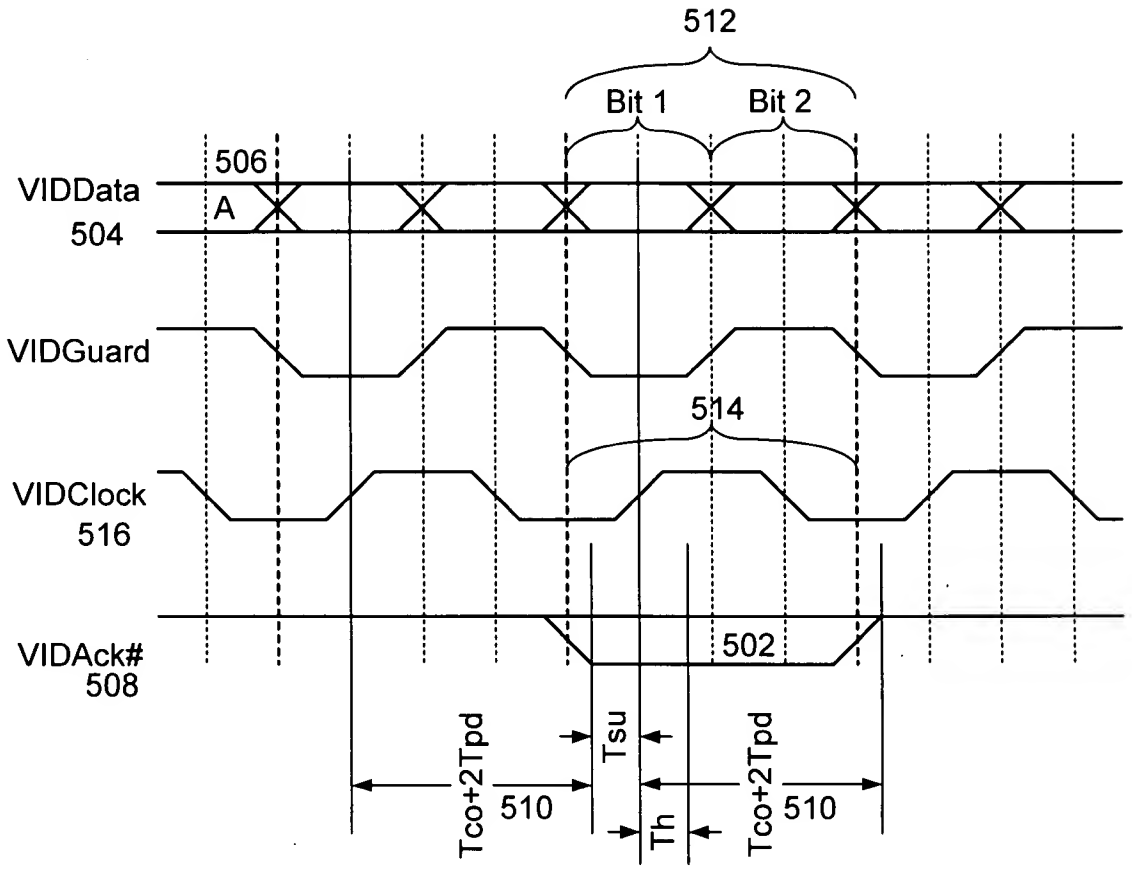

Fig. 5

SM Bus

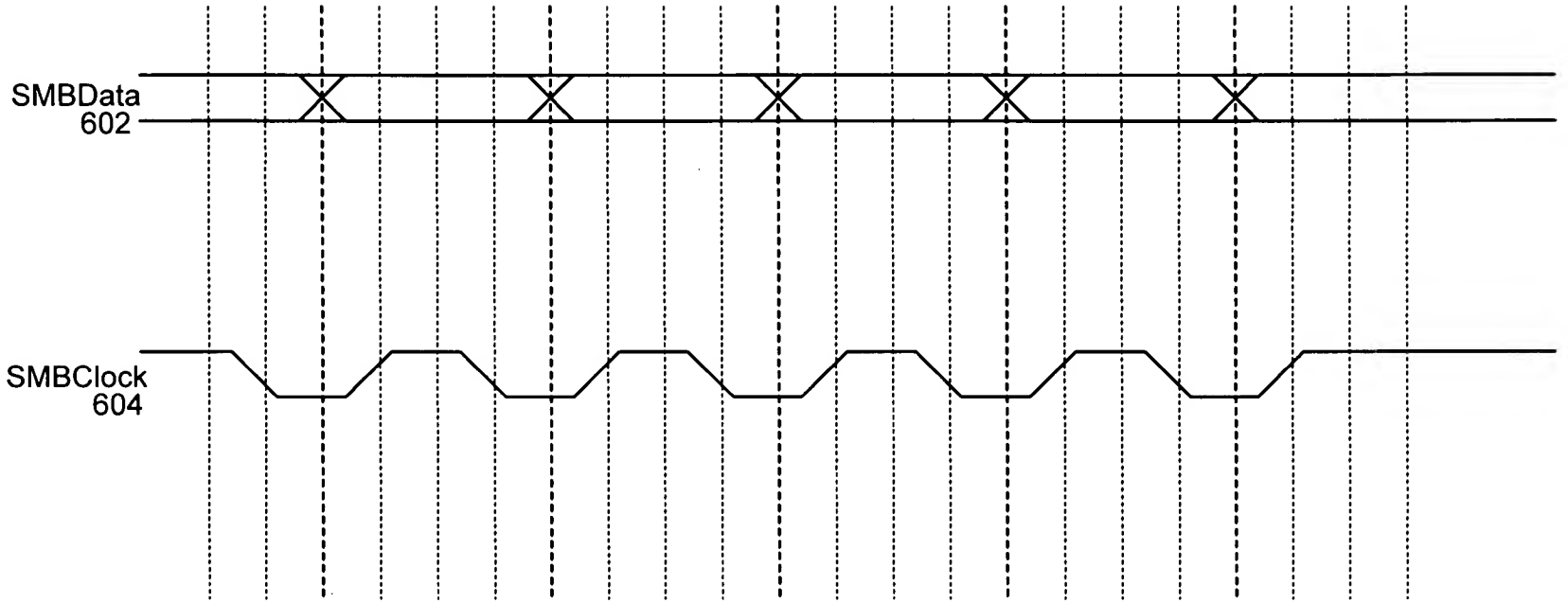

Fig. 6
Prior Art

Command Byte

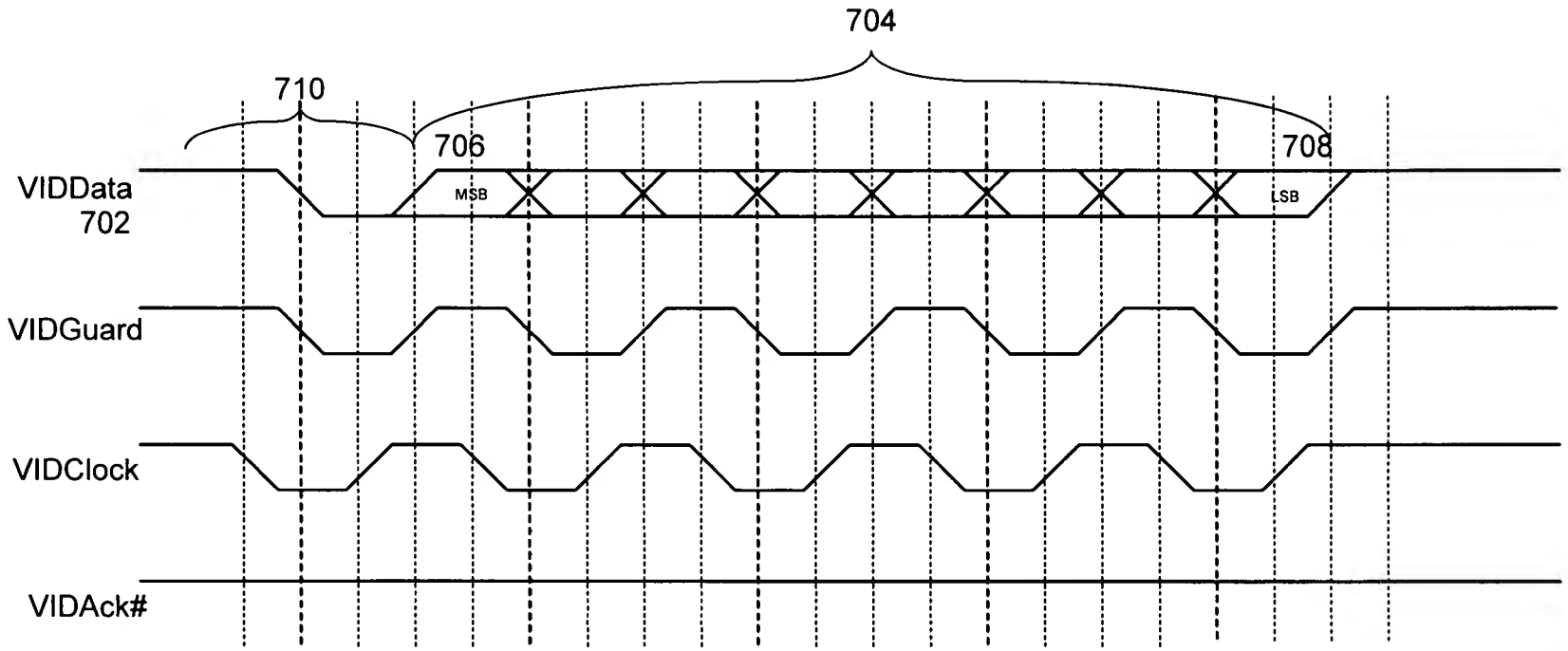

Fig. 7

Data Out Byte

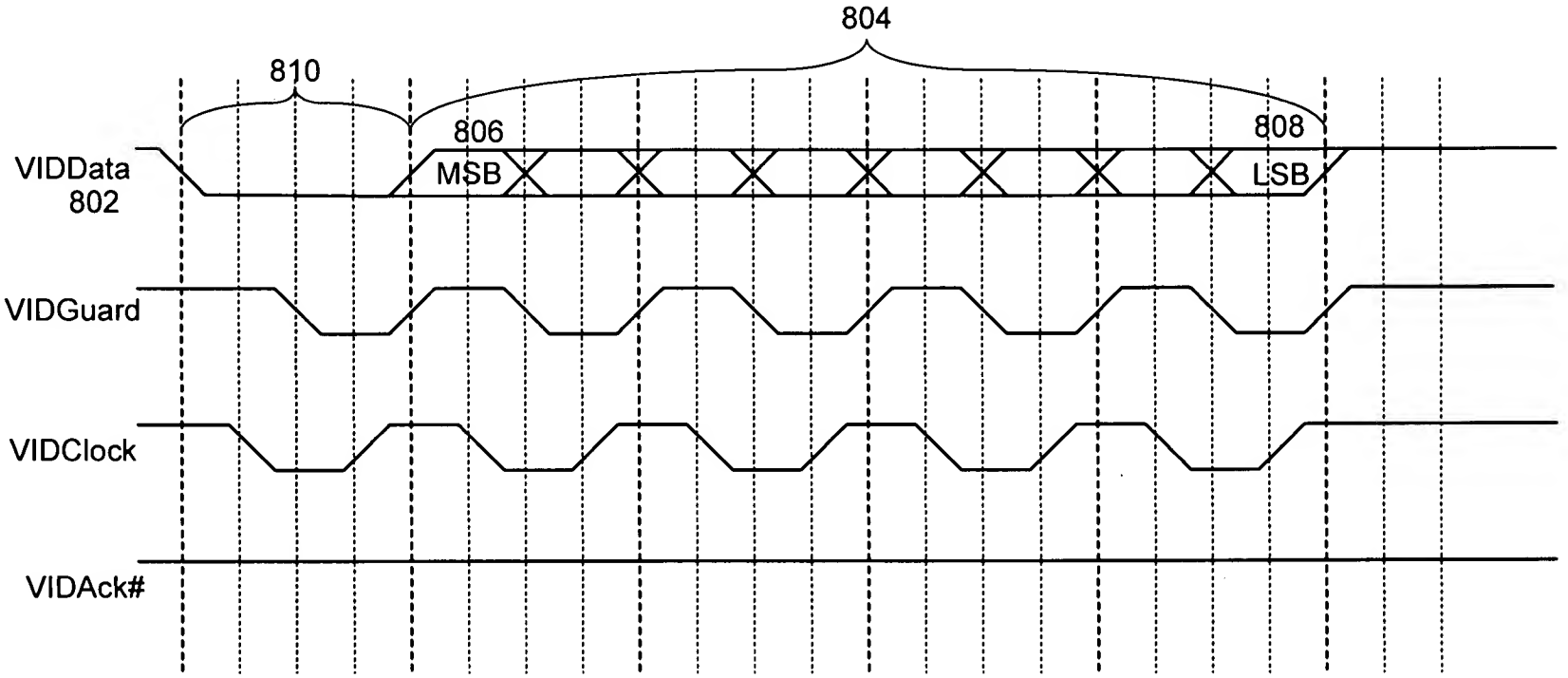

Fig. 8

CRC-8 Byte

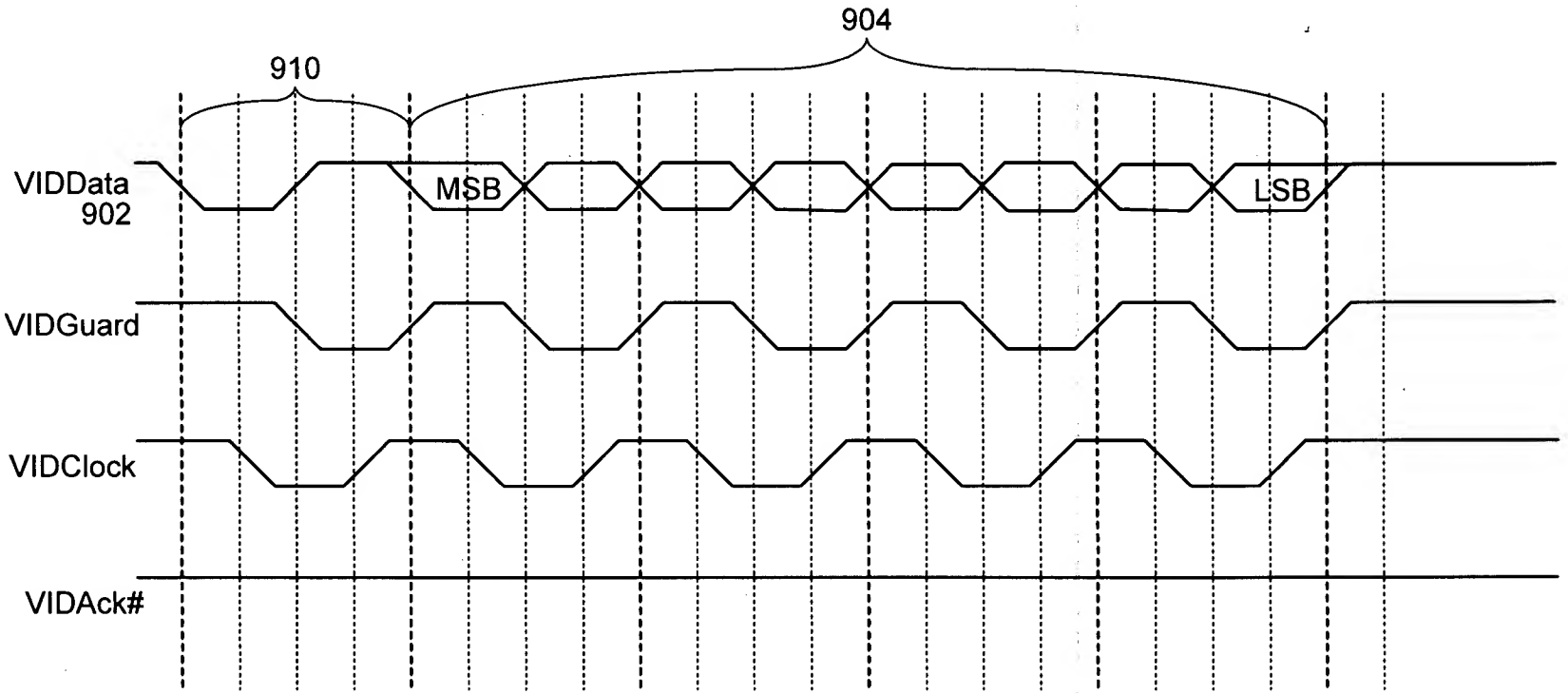

Fig. 9

Ack Byte with Positive Acknowledgement

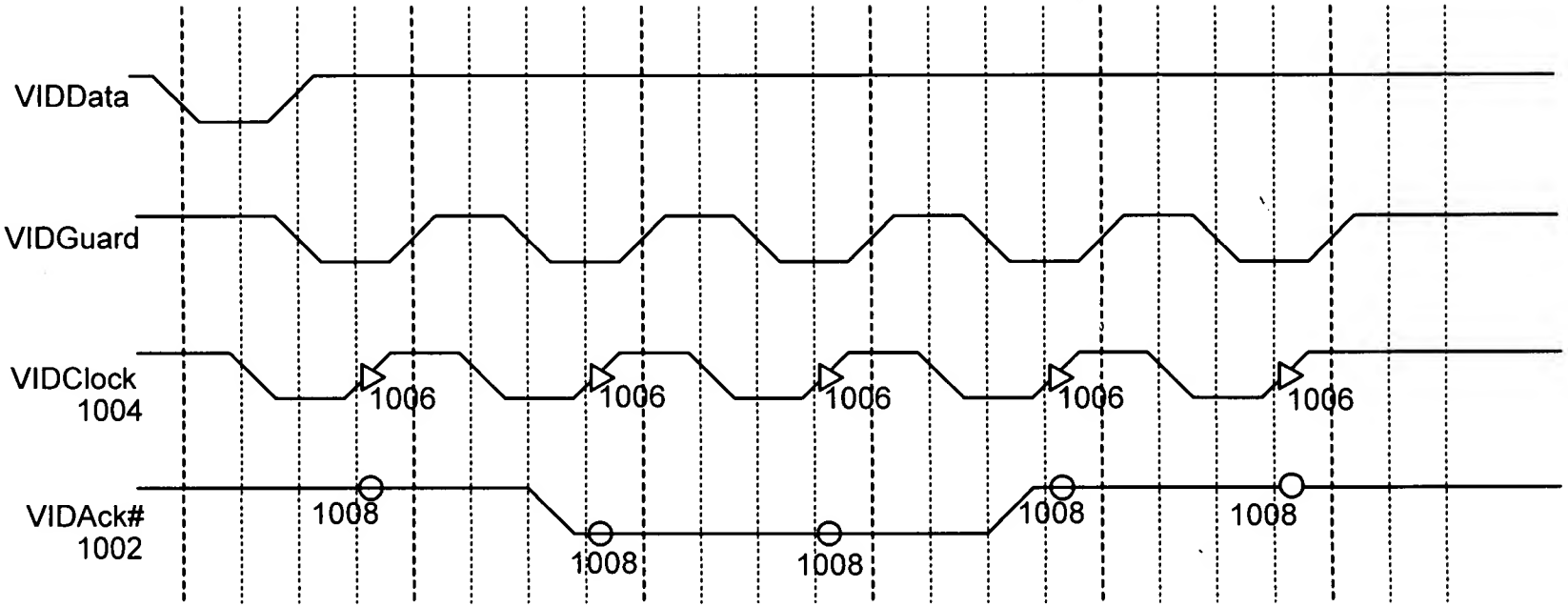

Fig. 10

209TTO 29056860

Sync Byte

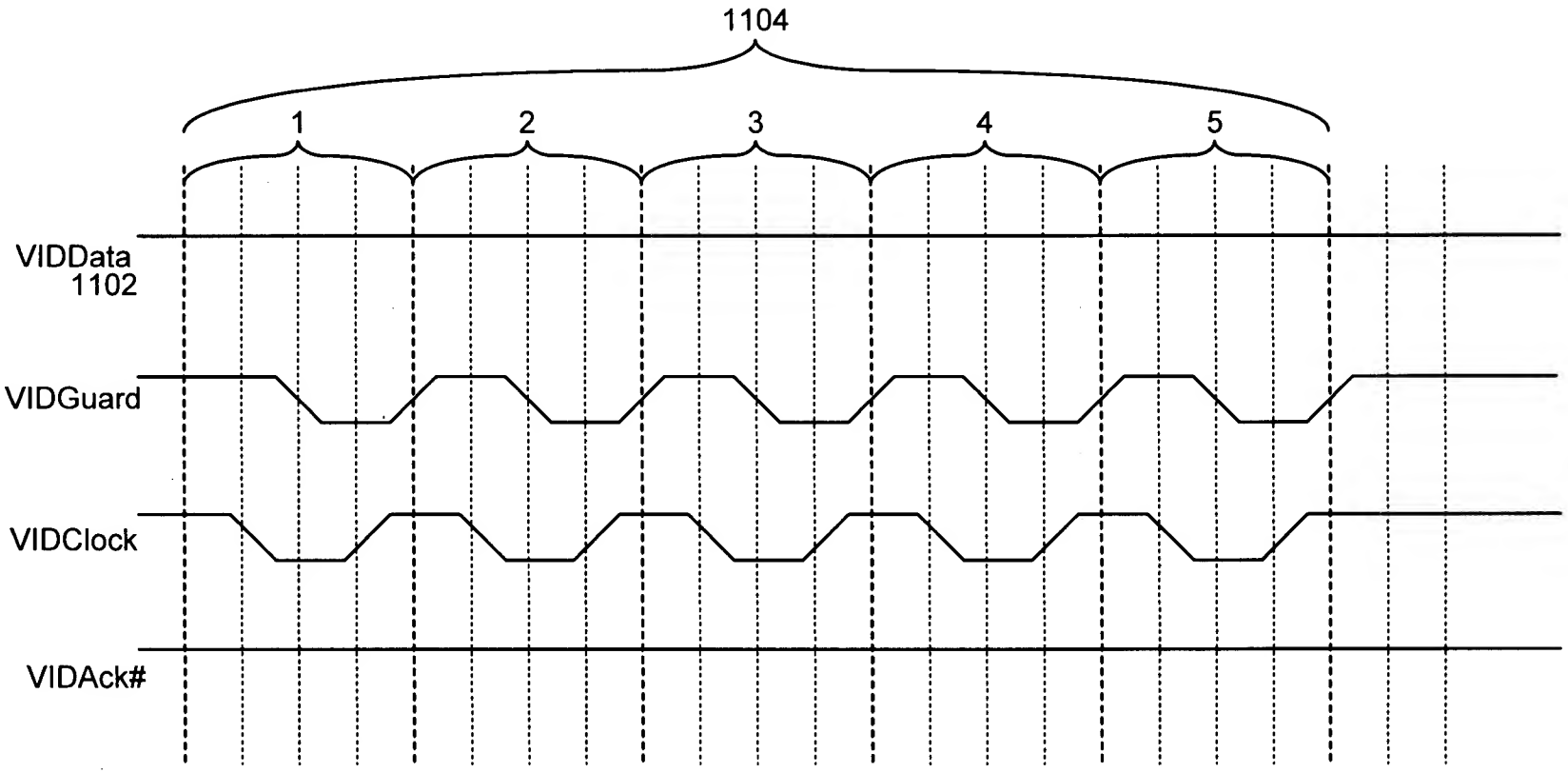

Fig. 11

Complete Command

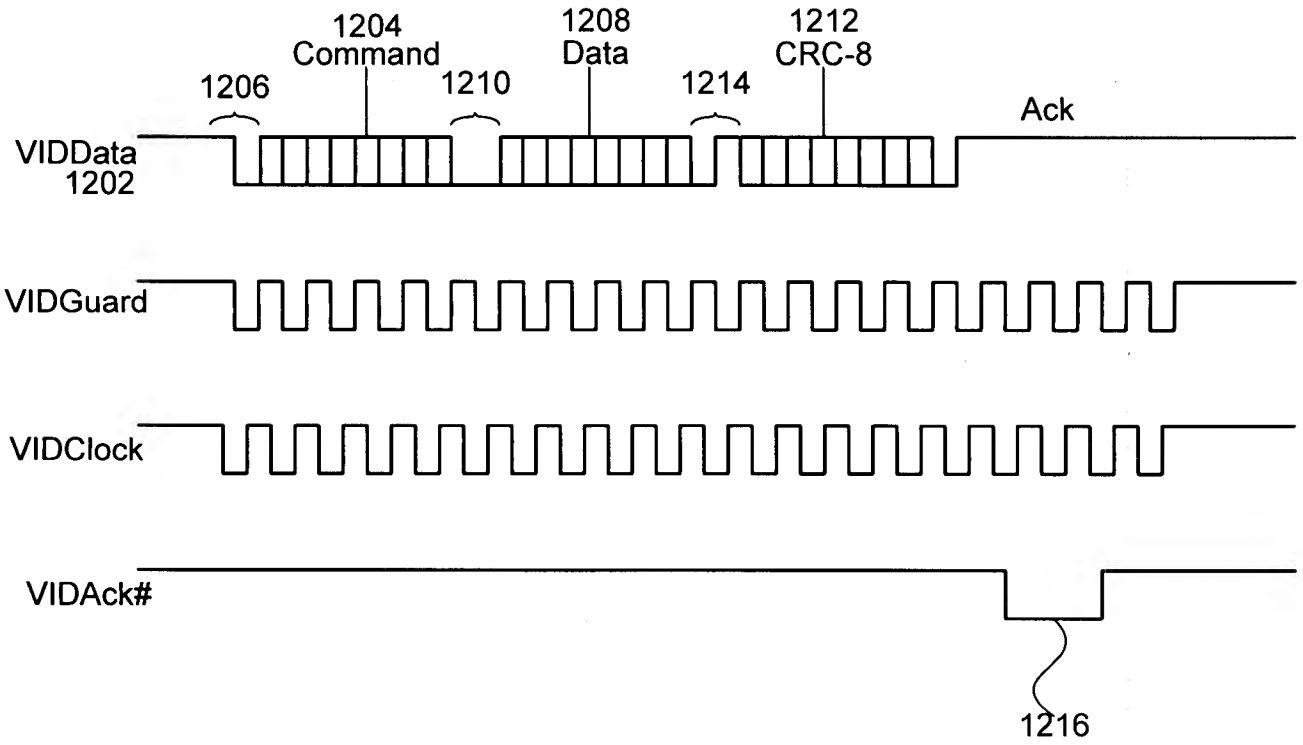

Fig. 12